ABSTRACT OF THE DISCLOSURE

A process for determining the optimum load driving capacity for each driving node in a complex logic circuit is disclosed. First, the logic equations of the logic circuit are extracted from a circuit description. Then, the fan-out of each driving node is analyzed to determine if the total number of pass transistor loads of the analyzed node is excessive compared to a predetermined driving capacity. For each flagged node, logic equations are added which represent the sum of the node's pass transistor loads, and further logic equations are added to compare the number of pass transistors turned on from one to the absolute maximum for the node. Then, a formal proof program is used to analyze the logic circuit and determine which of the comparators have a true output. For each flagged node, the comparator for the largest number which has a possible true output is identified to determine the highest possible actual load for the node; and, if necessary, the driving capacity of the node is adjusted to handle the determined highest possible actual load.